Peregrine Semiconductor

Bringing RF Tunability to Mobile Communications Markets

3-Dec-10

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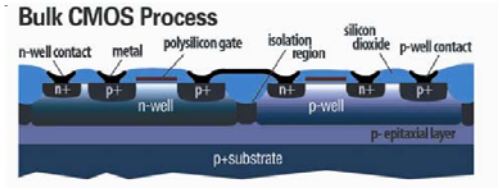
Outline

- Brief Introduction to Peregrine Semiconductor and UltraCMOS™
- Tunability Defined
- Antenna Frequency & Impedance Tuning
- Amplifier Multi-Mode Operation
- The Power of CMOS Integration
  - Power Control
  - Digital, Analog, RF
- Conclusion

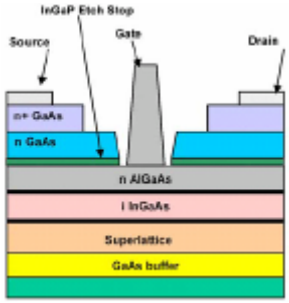
UltraCMOS™ Integrates Best In Class Performance

Bulk CMOS



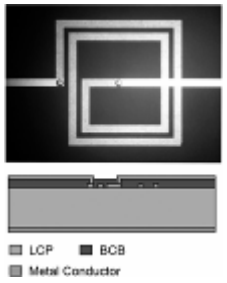
- Monolithic Integration
  - Manufacturable
  - Transferrable
  - Repeatable
  - Scaleable

Gallium Arsenide



- RF Power Applications
  - Good linearity
  - High mobility
  - High power handling
  - Good isolation

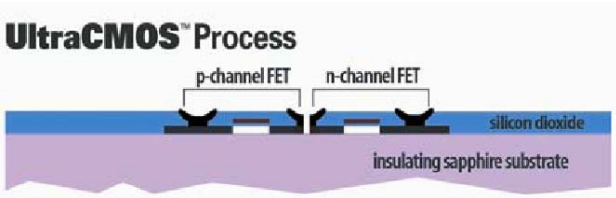
Integrated Passive Device



- Passive Integration
  - Miniaturized passive blocks
  - Minimized parasitics
  - Lithographic interconnect

UltraCMOS™

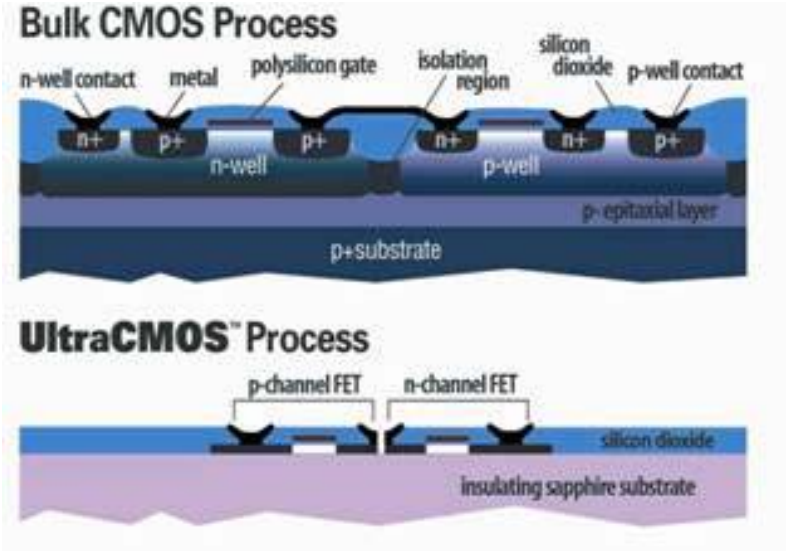
- All positive attributes of CMOS
- All positive attributes of GaAs
- All positive attributes of IPD
- Additional Unique Properties

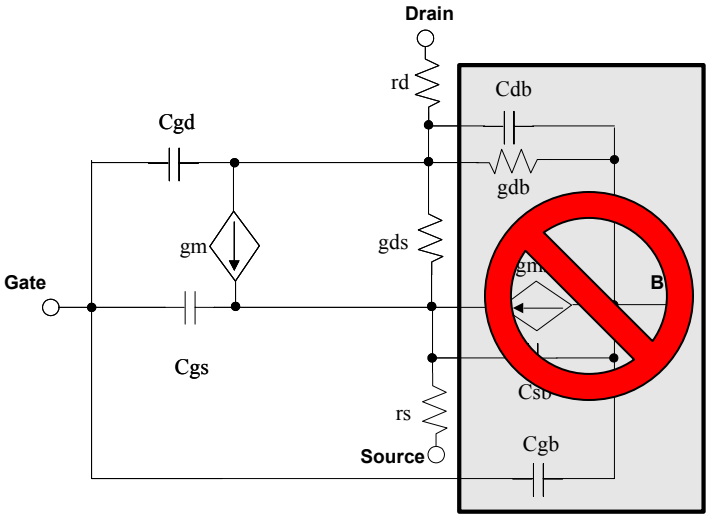


- + Broadband Linearity
- + Unprecedented Isolation
- + High ESD Handling
- + Onboard Memory - EEPROM

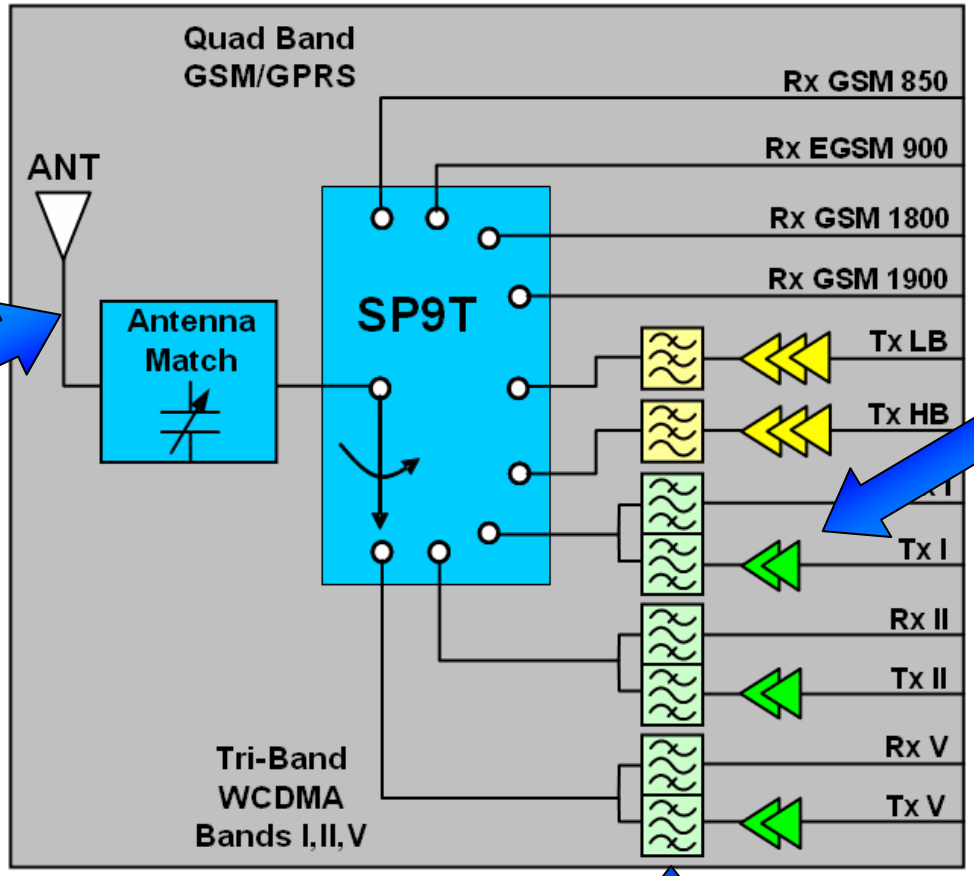
UltraCMOS™ - The Ultimate RF CMOS Technology

- The sapphire substrate eliminates the bulk parasitics!
  - **Fast** devices
  - **Ultra low power** loss
  - Excellent **linearity**
  - Unprecedented **isolation**
  - Ability to integrate **high Q passives**
  - Ability to integrate multiple **RF / mixed signal / digital** functions monolithically





Tunability Defined – 3G Handset Architecture



Antennas
- Frequency
- Impedance
- TRP/TIS

Amplifiers
- Frequency
- Mode
- Power & PAE

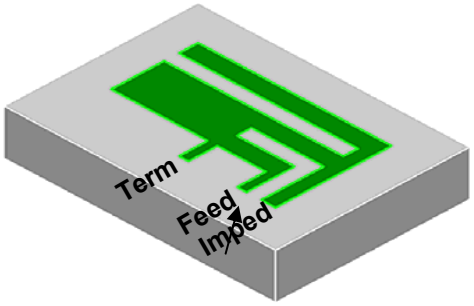
Filters
- Pass Band
- Notch Frequencies
- Insertion Loss, Rejection

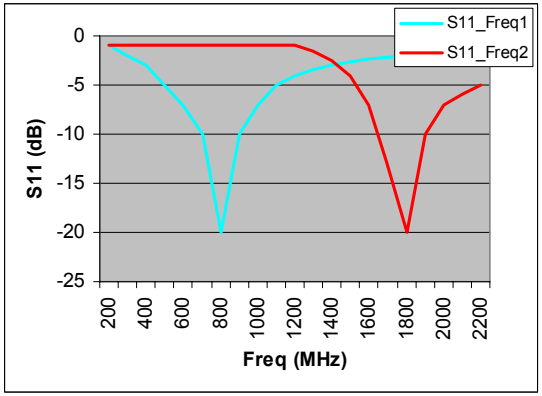
Why Tunability?

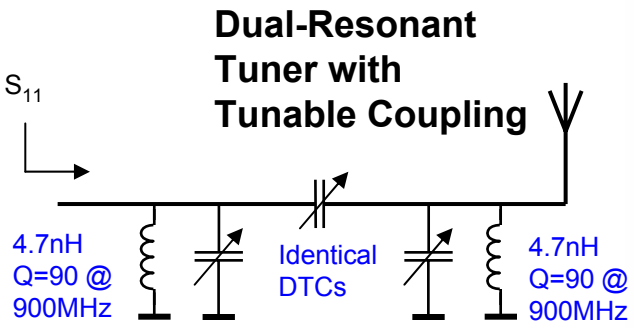
- The Number of Handset Frequency Bands continues to increase
  - Moving from 2G Quad Band to 3G/4G 7-12 band Smart Phones
  - Drives the complexity and increases the number of discrete, fixed frequency components
- Tunability helps reduce the total Bill of Material
  - Multiple Antennas, PAs, Filters are replaced with fewer, tunable elements
- Reduce total board area with fewer components
- Tunability leads to improved communication link performance
  - Improved TRP & TIS leads to lower BER, fewer dropped calls
- Improve battery talk time
  - Antenna impedance matching is the most straightforward means to improve TRP by >3dB
    - The PA Power savings drops directly to the talk time “bottom line”
  - Improve Tx efficiency level over entire PDF

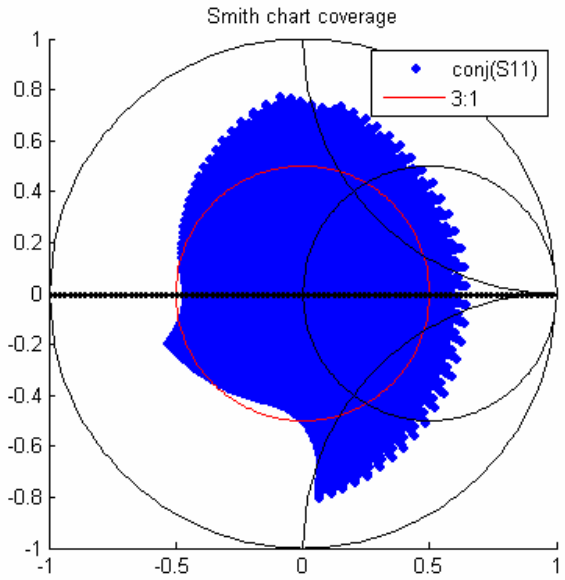
Antenna Frequency and Impedance Matching

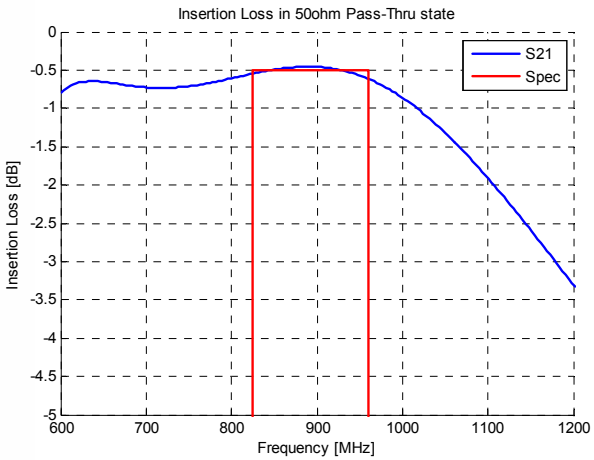
- Frequency Tuning of a PIFA Antenna with an Variable Loading Impedance
  - Single antenna with minimal volumetric size can address multiple bands
- Impedance Matching of Antenna to address EM Proximity Effects



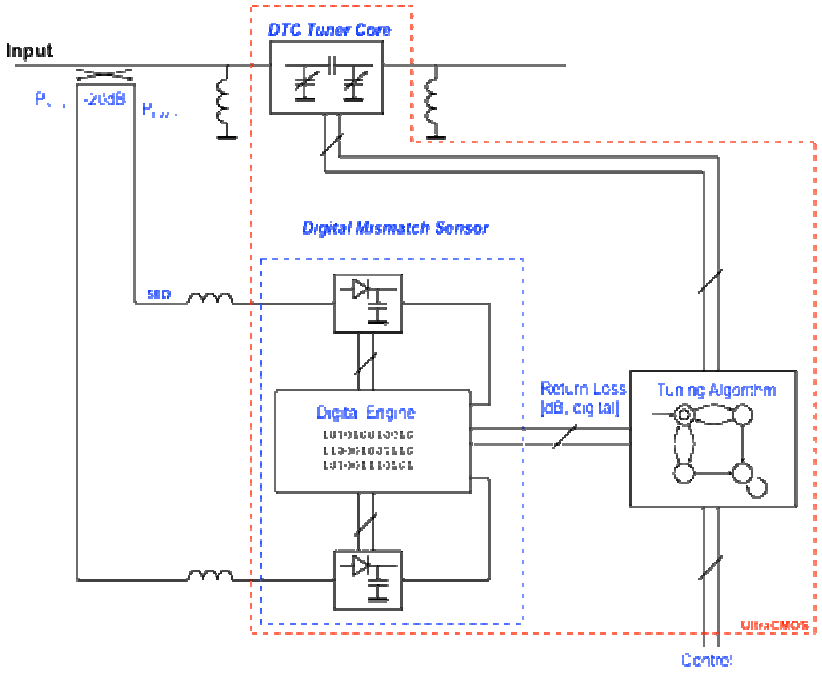








RF Front-End Mismatch Loss Tuner



Pro's and Con's

- Improves static and dynamic mismatch loss
- Complex system design
- Requires close co-operation with handset/network provider to implement solution

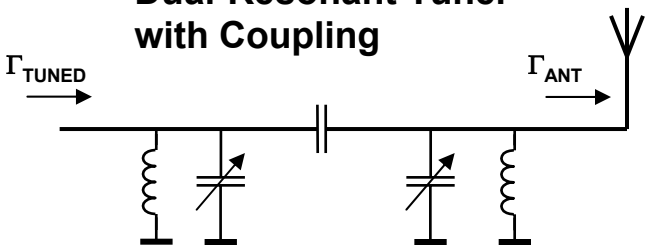
Implementation and Control

- RF Front-end mismatch tuning device controlled by a closed loop mismatch sensing device and tuning algorithm
- The sensing and tuning algorithm can be implemented several ways
  - Fully autonomous subsystem – turn it on and it tunes
  - Controlled by BB/DSR core processor chip

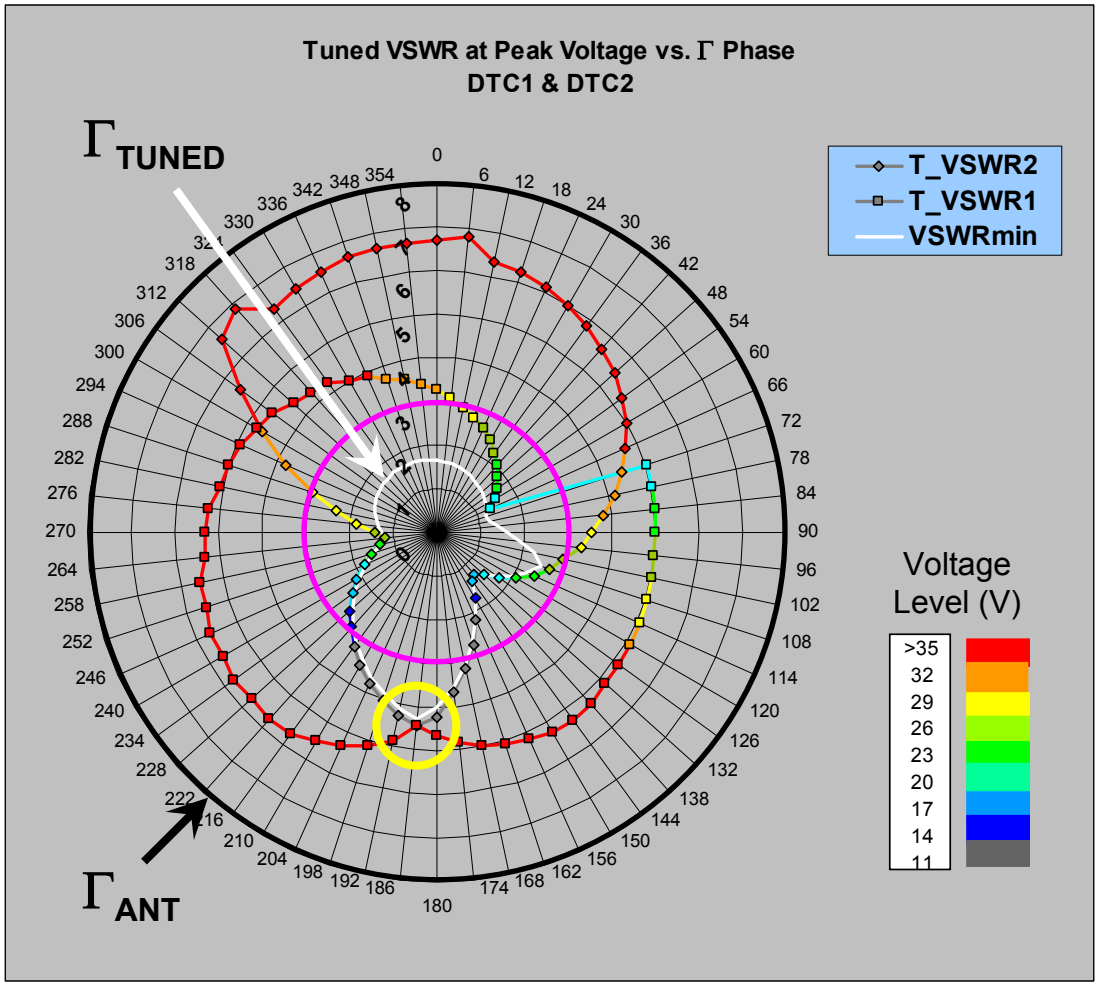
Added Design Complexity and Constraints

- With Tunability come new design challenges
  - e.g. Avoid High Voltage conditions over impedance tuning range
    - Linearity
    - Reliability

Dual-Resonant Tuner with Coupling

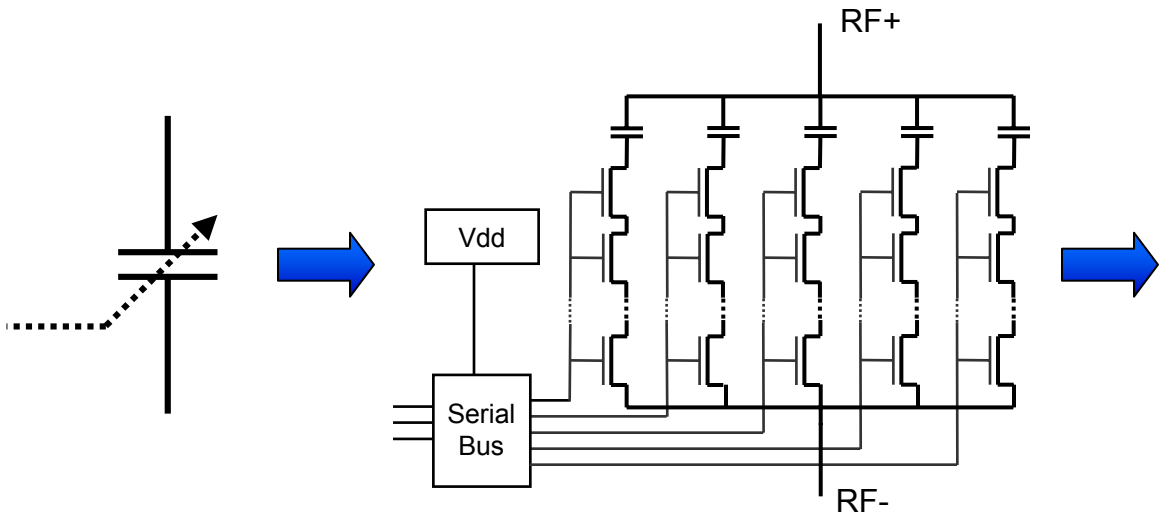


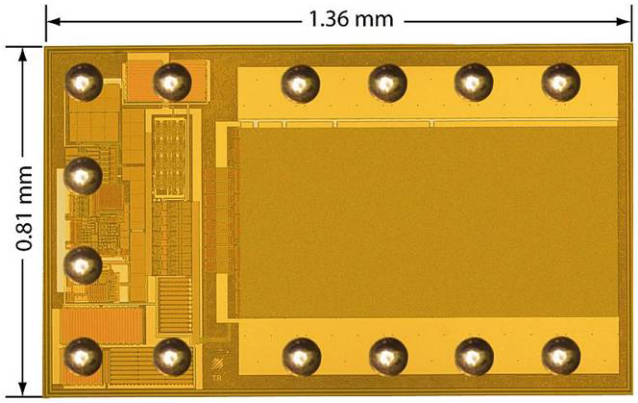
8:1 Antenna Impedance Γ_{ANT} Matched to Γ_{TUNED}



+34dBm P_{INC} @ 900MHz

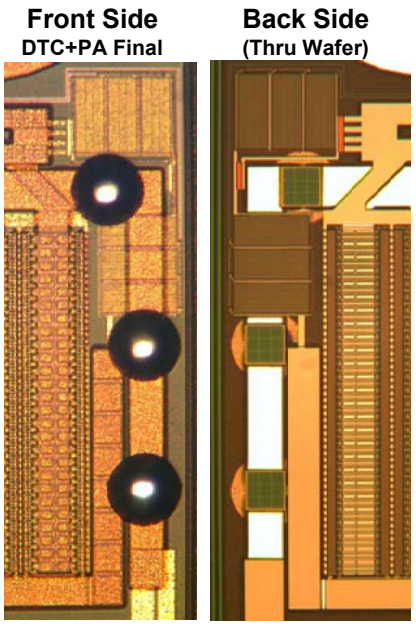
Core Element - Digitally Tunable Capacitor





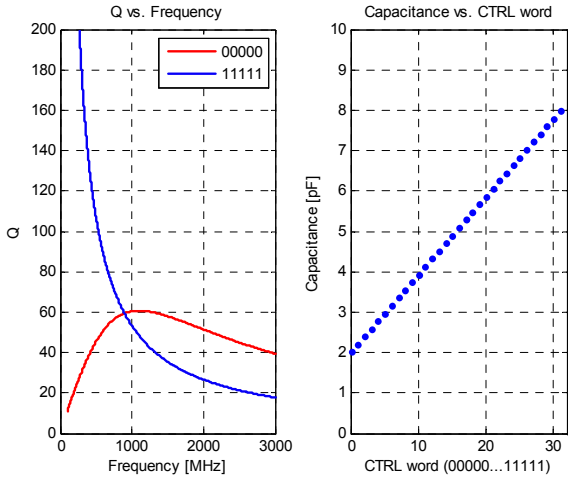
Device Features

- Single monolithic die
- Solid state implementation
- Direct connect to V_{BAT}
- Simple serial control interface
- Proven UltraCMOS™ process
  - >700M devices manufactured
- DTC can be directly integrated within more complex RFICs



Performance Attributes

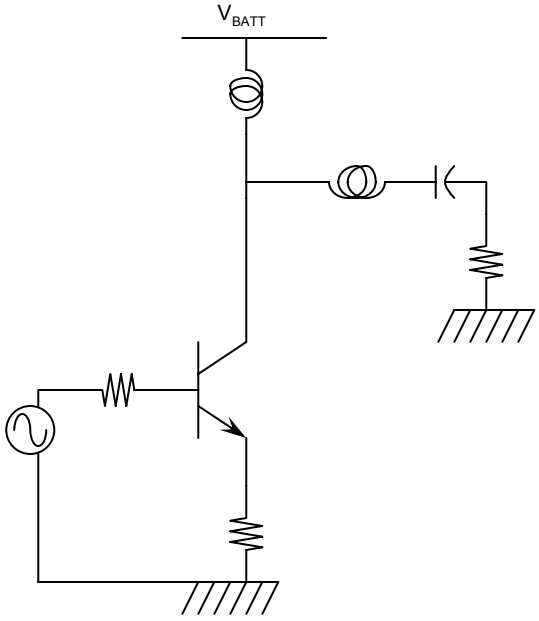
- Tuning range of 4:1
- Capacitor range 2pF to 8pF
- Typical Q = 60 @ 1GHz



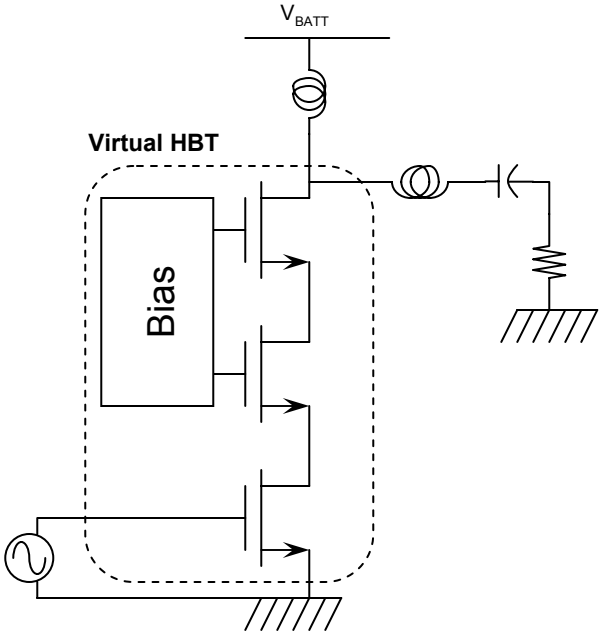
Creating the 'Virtual HBT' in UltraCMOS

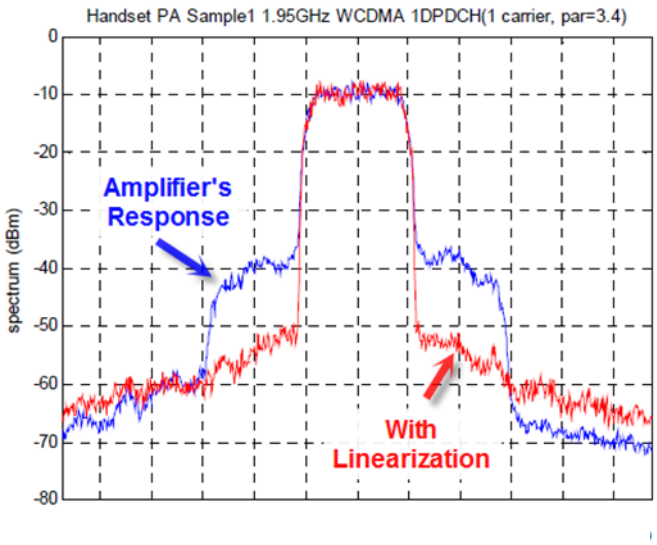
- Using device stacking, a virtual high-voltage three-terminal device can be realized
  - Can be operated in either linear or switched mode
  - Complex control and linearization schemes can be implemented
    - Analog, Digital linearization/pre-distortion techniques

HBT PA Implementation



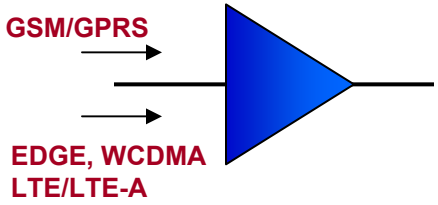
CMOS PA Implementation

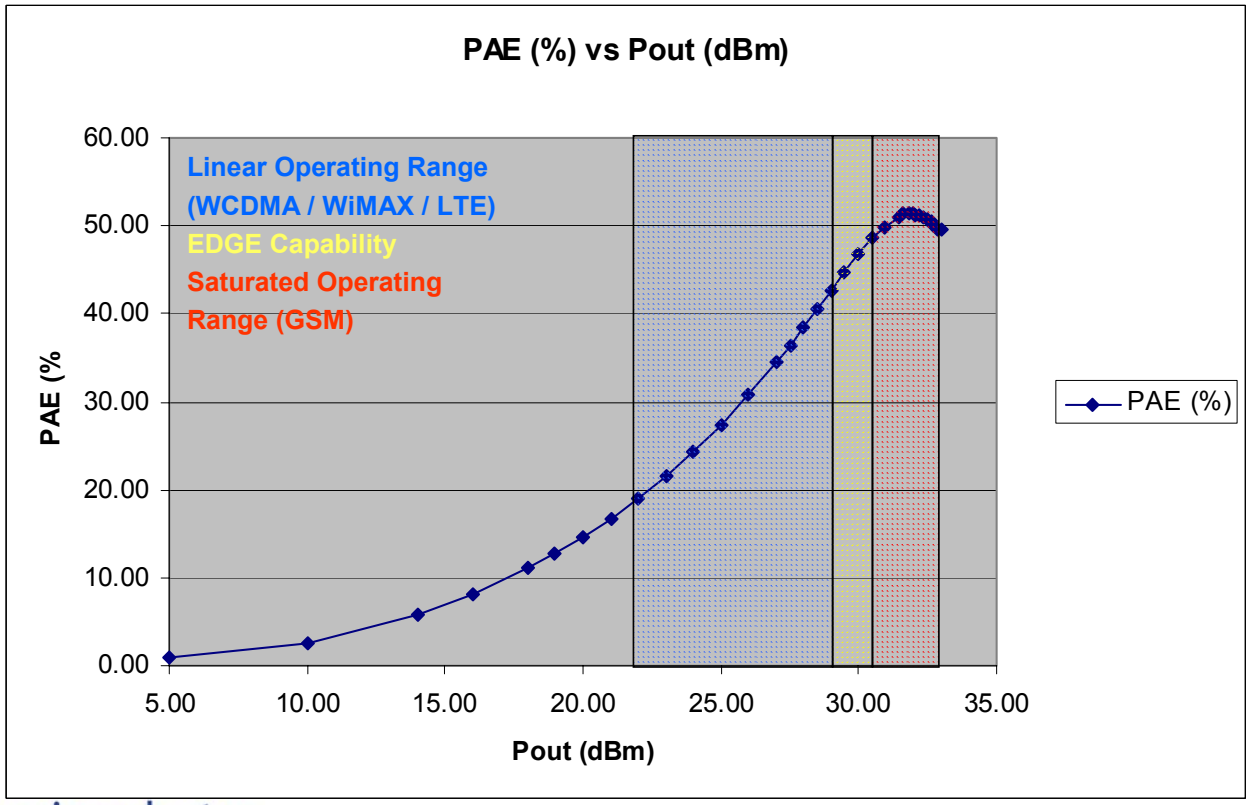




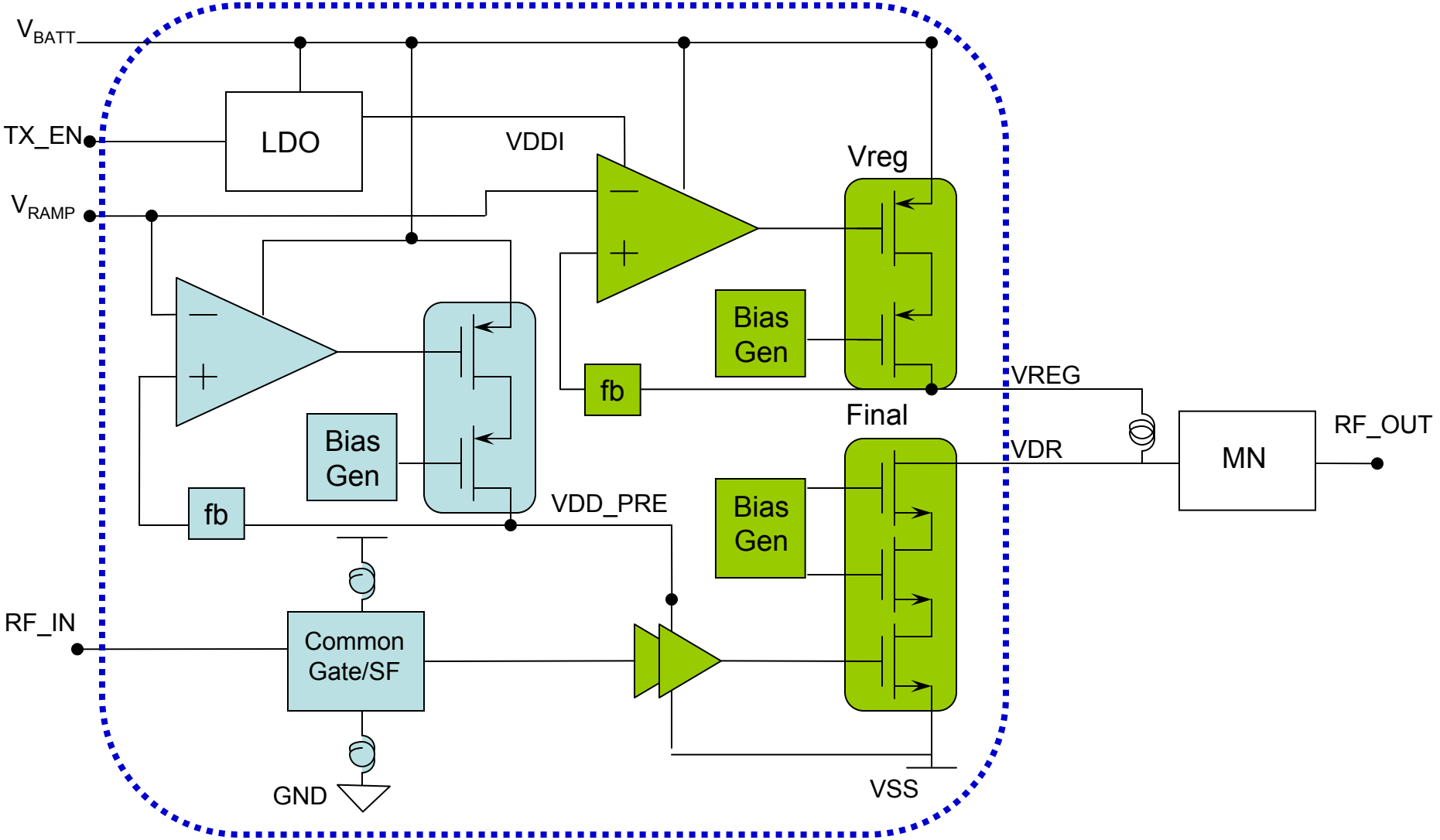
Power Amplifiers – Switched & Linear Synergy

- Critical to reducing the number of power Amplifiers is Multi-Mode Operation from a single amplifier
  - Constant Envelope versus high Peak-to-Avg Ratios (PAR)
- Common Final Amplifier Stage Performance
  - Pout & PAE performance maintained across multiple access schemes



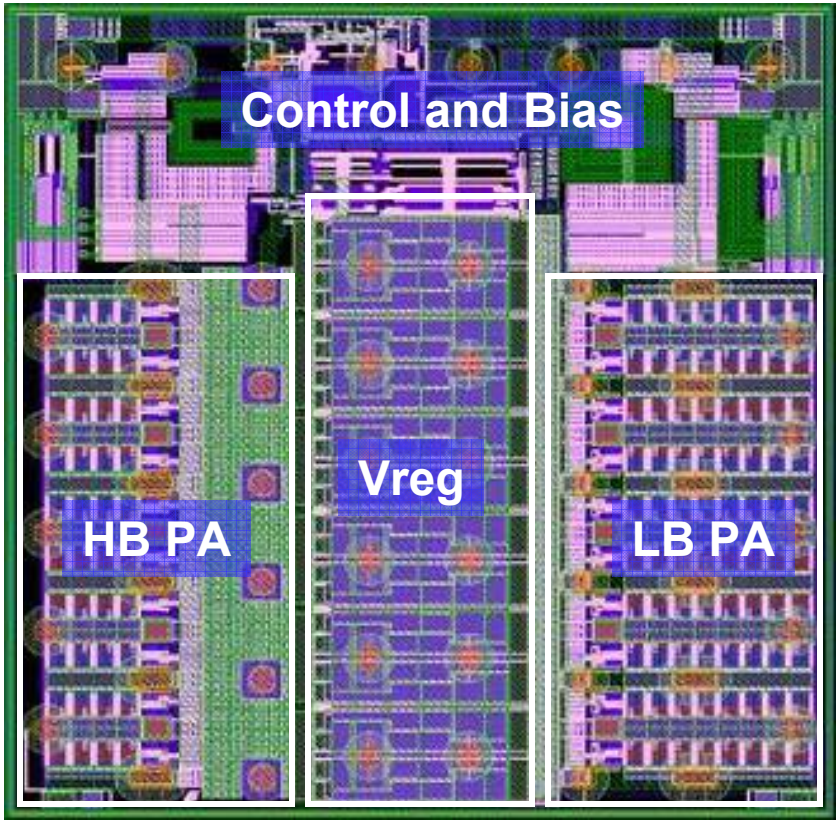


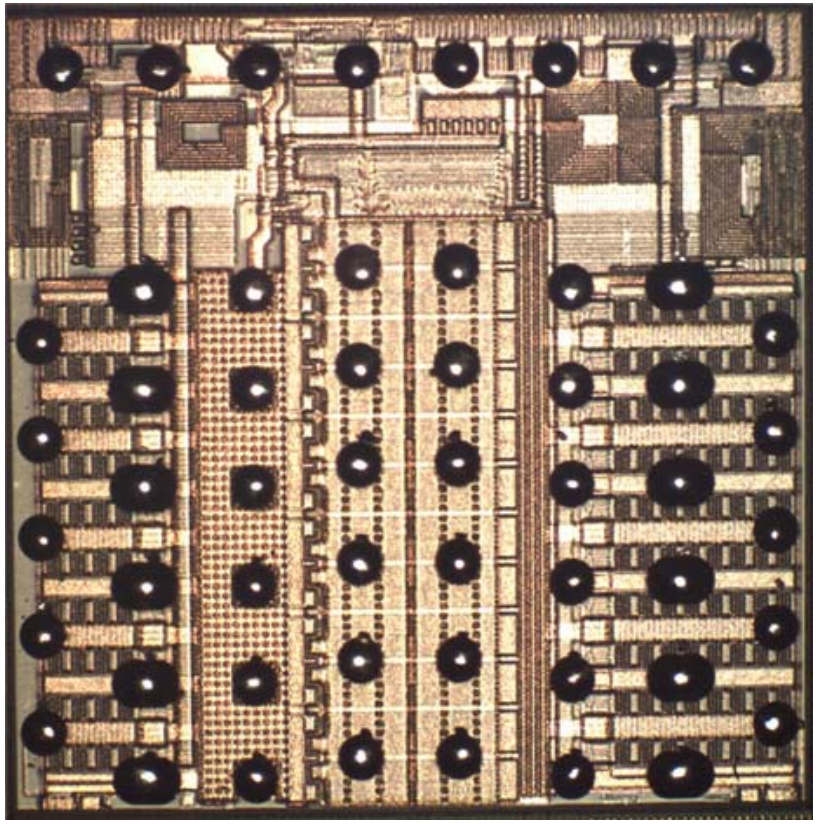
Complete Integration of GSM PA with Controller



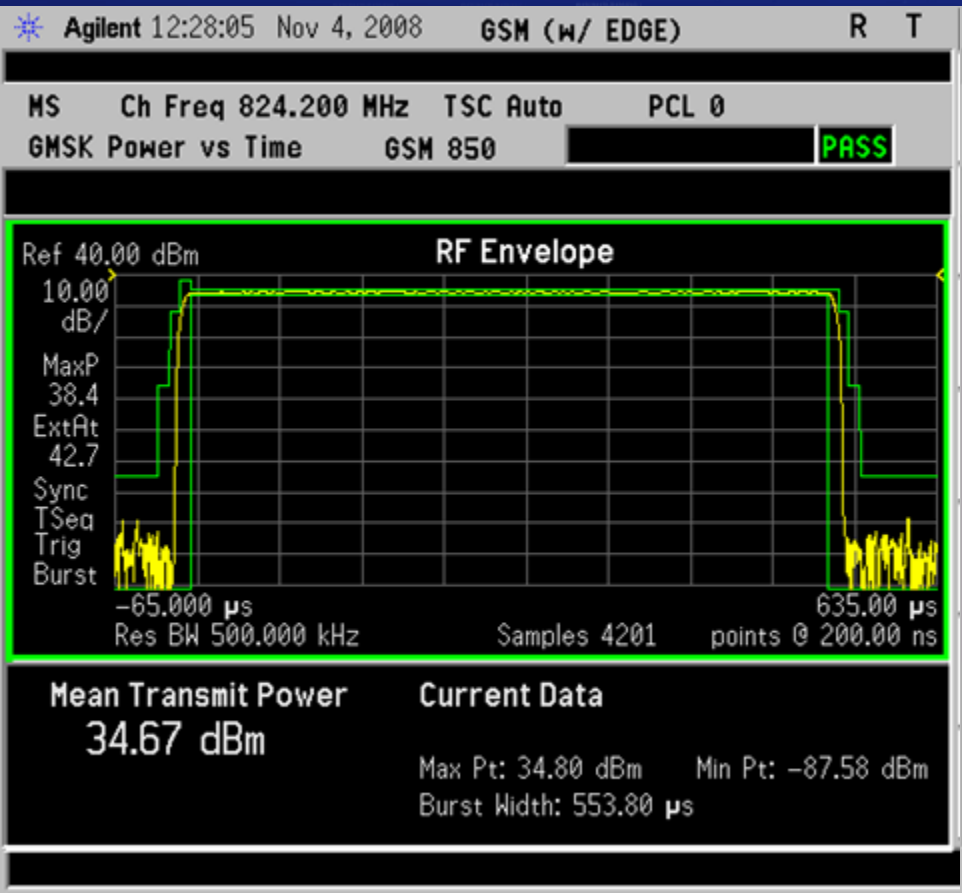
Physical Implementation

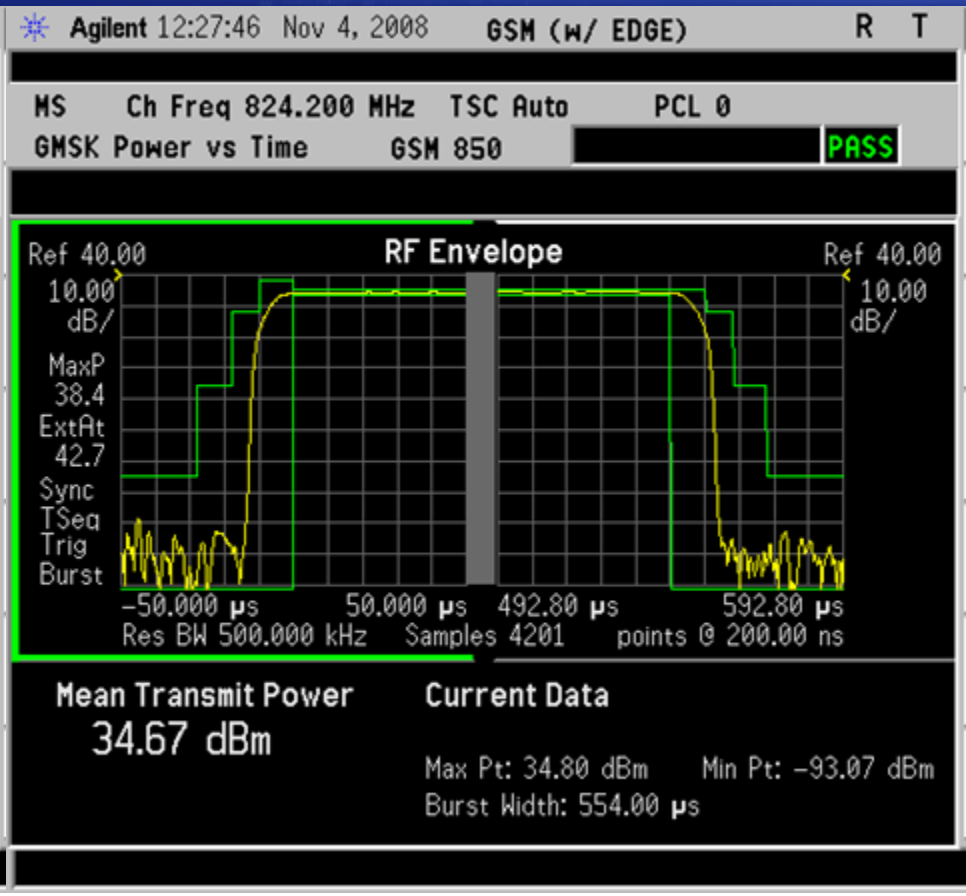
- Monolithic Integration of the GSM APC function
- Rugged into any load condition at max power





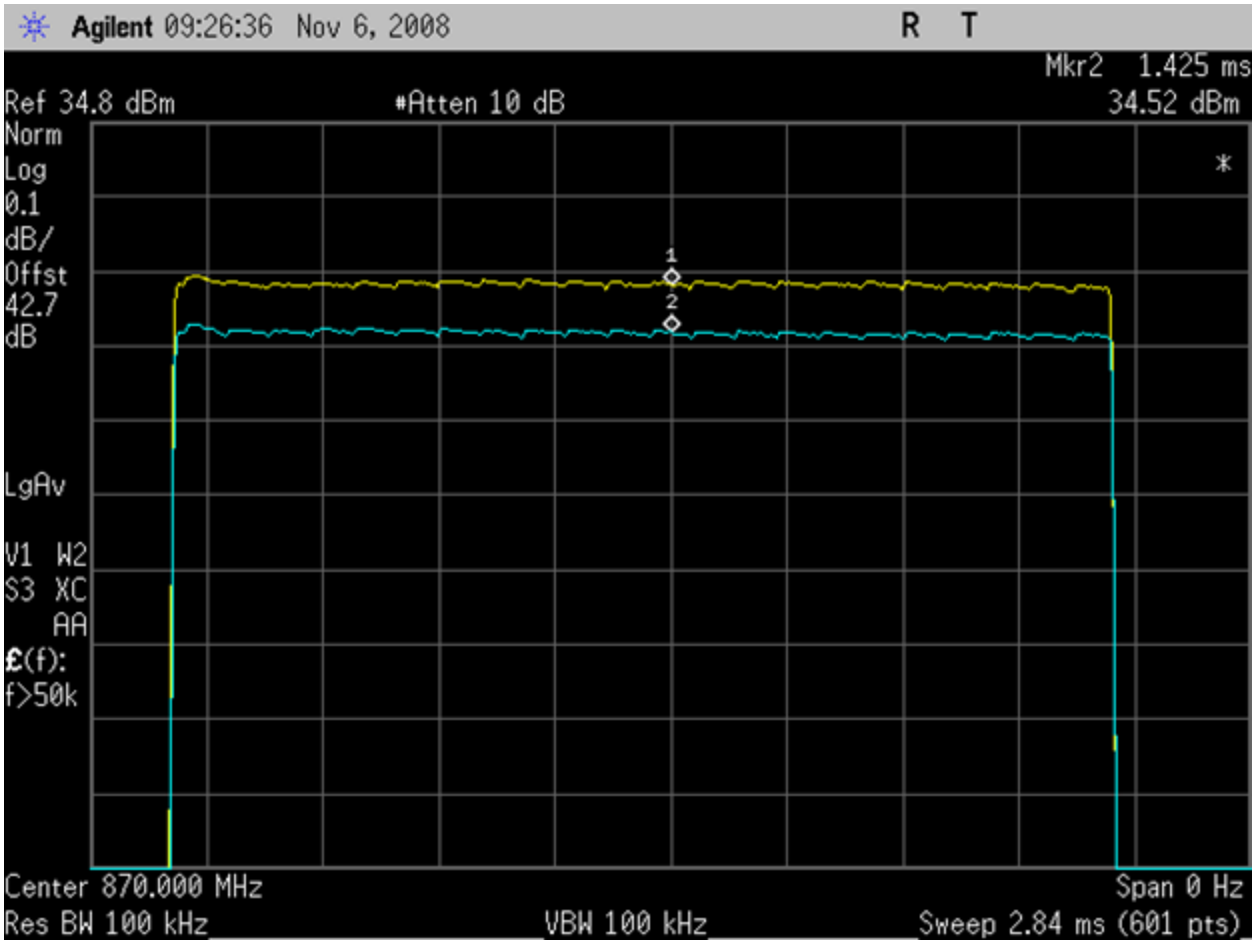
GSM 850 – Power vs. Time @ 3 V Vbatt





- **Large power control range > 75dB**
  - Tx/Rx Switch doesn't have to be sequenced to meet the time mask
- **Well behaved analog power control**
- **Very repeatable results – multiple parts/multiple wafers**
  - Over frequency and V_{BATT} range

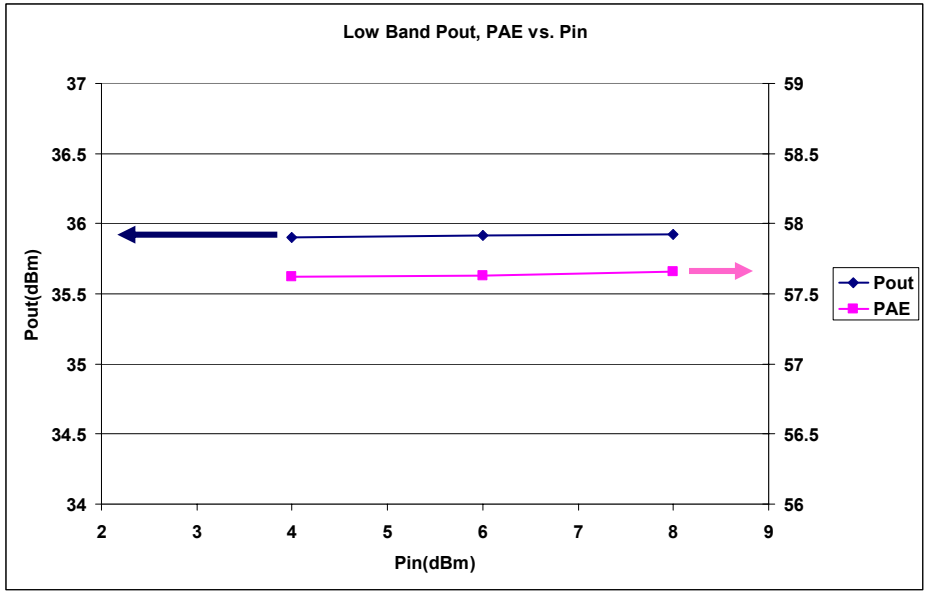
GPRS Class 12 (50%) Operation

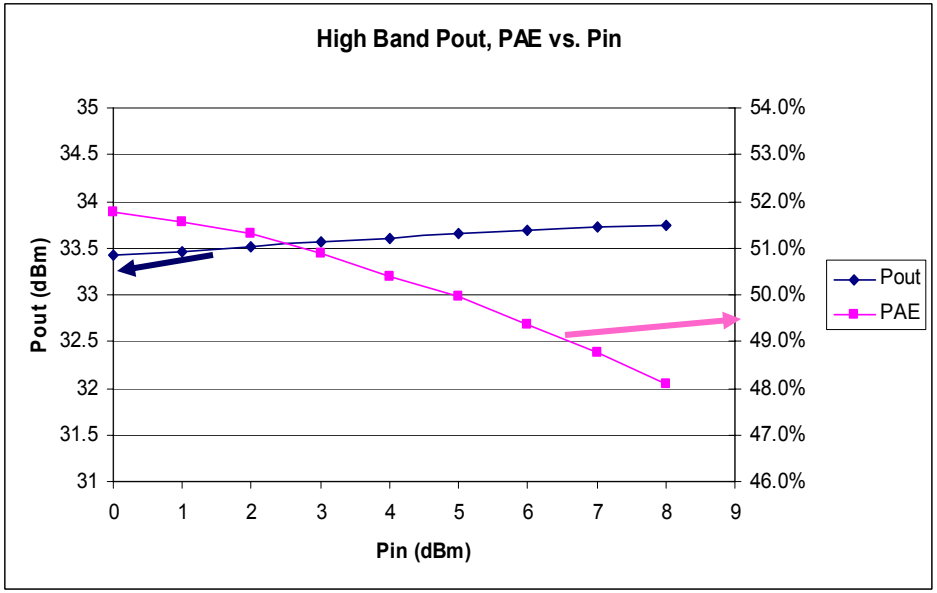


Marker1 (Yellow Trace) @ Start = 34.58 dBm
Marker2 (Blue Trace) @ 5 minutes Later = 34.52 dBm

Delta = .06 dB

Output Power & Total Efficiency vs. Pin



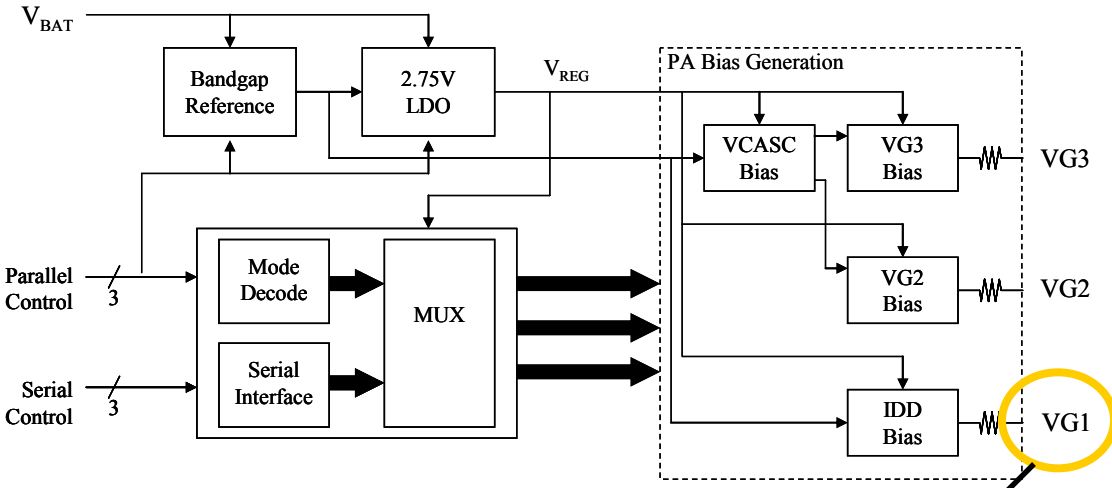


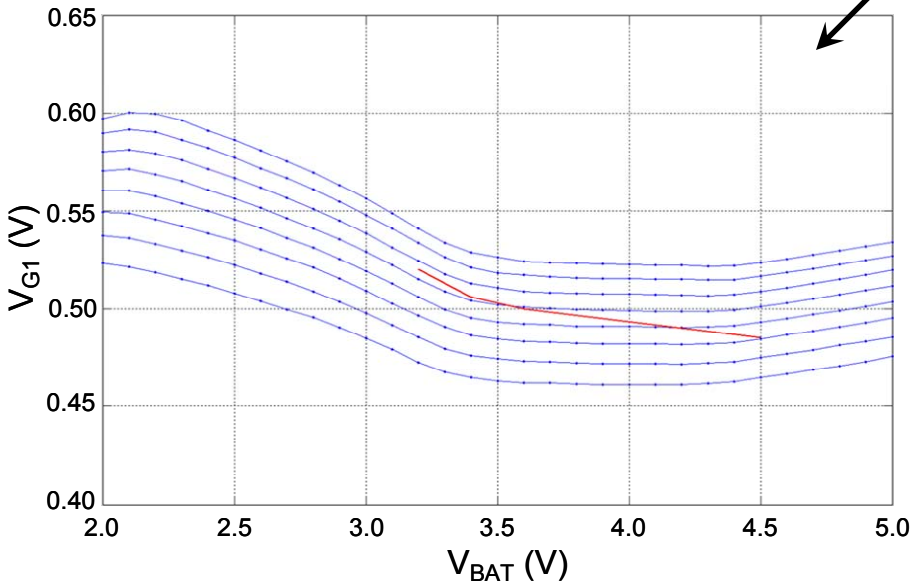
Measurement Conditions: Freq.=880 MHz, 1780MHz
V_{BATT}=3.5V, V_{RAMP}=1.7V

- **Outstanding Efficiency (best CMOS results, competitive with GaAs)**
- **Plenty of Output Power**
- **Pout independent of Pin**
- **Low Pout dependence on Temperature and V_{BATT}**

WCDMA Linear PA Bias Generation

- Provides optimum linearity performance
  - ACLR, IP3
- Minimizes performance sensitivity to Process, V_{BATT}, and Temp Variations
- Relies upon proven CMOS Analog & Digital design concepts to optimize operating points based upon PVT





Conclusion

- Peregrine UltraCMOS has demonstrated tunability that addresses:
  - Frequency band switching
  - Impedance matching
  - Output power optimization
  - Access scheme/mode of operation
  - Tuning for environmental effects
    - Proximity effects
    - Temp, Battery
- Integration of high performance RF with Digital and Analog circuitry is paramount to tunability
  - Qcap > 60, Qind > 30 for 1-2GHz
  - Ron-Coff Device FOM is continuing down CMOS scaling curve
    - 375 ➡ 275 ➡ 225 fS (1 Ohm-mm, 275fF/mm)
    - F_{MAX} 50GHz ➡ 100GHz