Components for Software Radio Wideband Receivers: A space segment survey

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Introduction

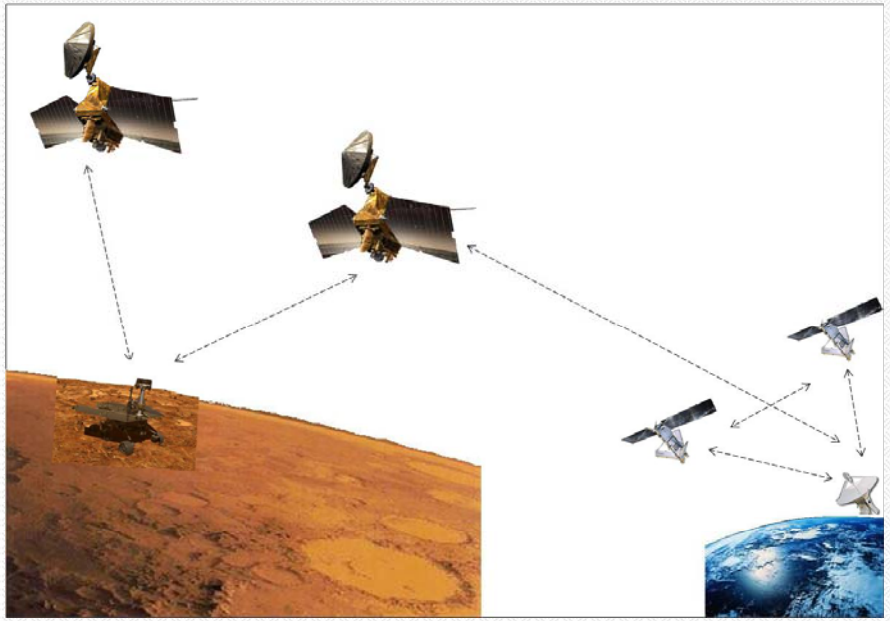
- Present and emerging scenarios for SDR space-borne applications
- Focus on three illustrated space missions
- Results from rad-hard/commercial-on-the-shelf ADCs survey
- Results from rad-hard/commercial-on-the-shelf FPGAs survey
- Conclusions

Present and emerging scenarios

- Design flexibility as optimal usage of in-orbit resources: communication payload and satellite subsystems.
- Advantages of the reconfigurable technologies: „pre-launch flexibility“, „post-launch flexibility“.

„Pre-launch flexibility“

„Post-launch flexibility“

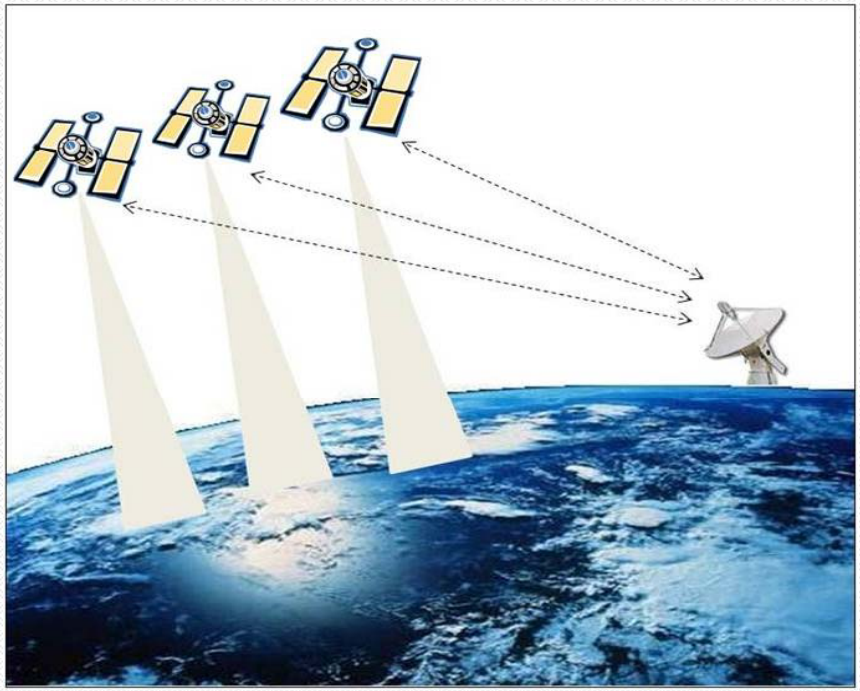


Three selected space missions

- TT&R subsystem for a GEO and LEO platform: AISCOMM, GEO-COM
- A RF inter-satellite link scenario for future satellite networks

GEO-COMM

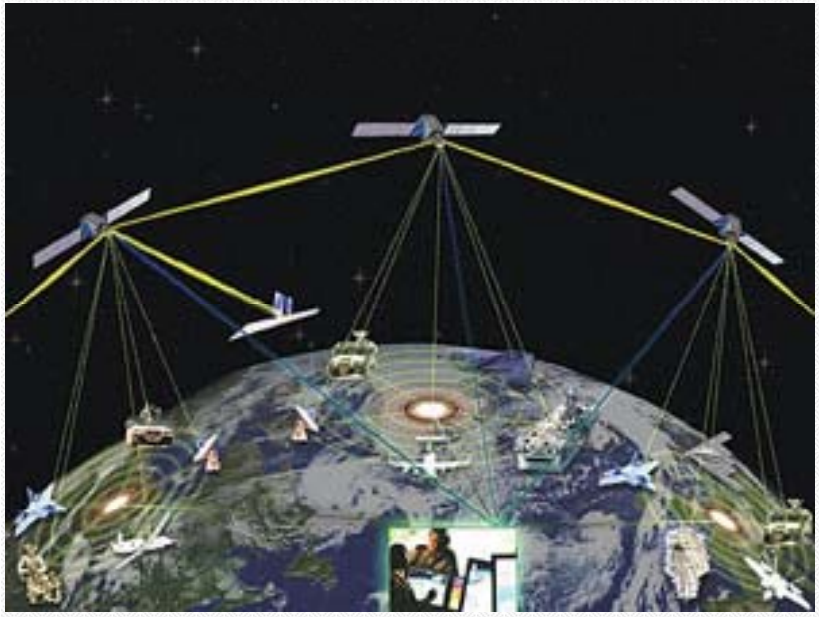
AISCOMM

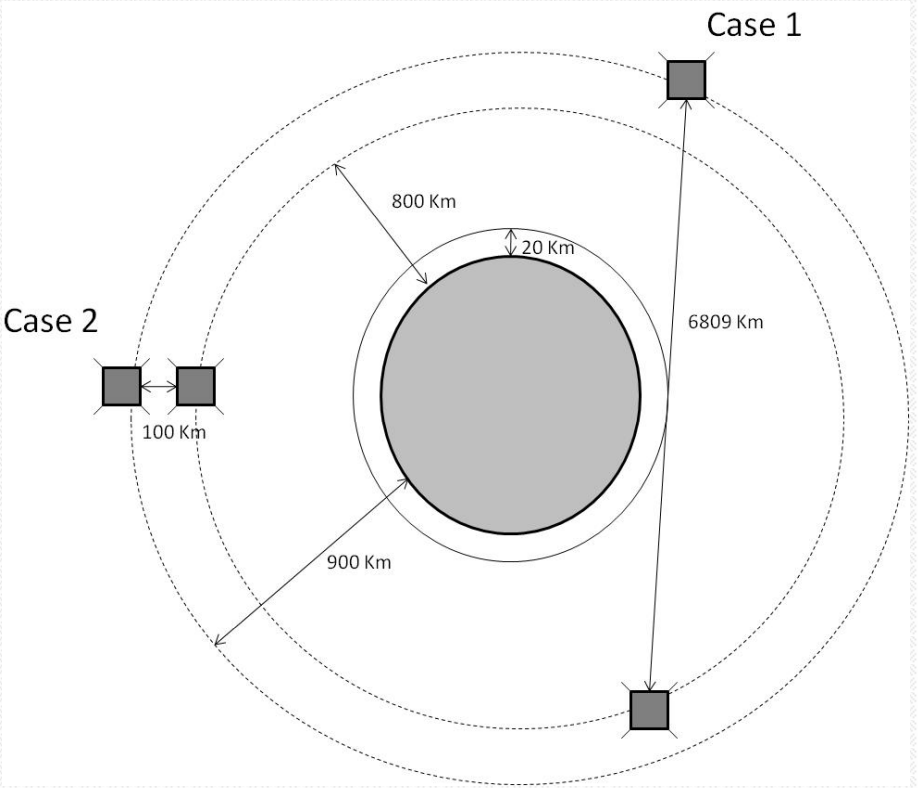


RF ISL scenario

ISL AIR INTERFACE FEATURES

Carrier frequency [GHz]	25
Data rate [Mbps]	150
Mod. Scheme	QPSK
LDPC coding rate	2/3
E_b/N_0 (on a frame of 43200 bits) [dB]	3
Filter Roll-off	0.4
Max Doppler freq. offset [MHz]	1.25
Bandwidth [MHz]	158.75





ADCs and FPGAs manufacturers

Analogue to Digital Converters

- Considered ADC in the survey: > 1 [Msps] of sampling speed
- Commercial ADC manufacturers: Analog Devices, National Semiconductors, Texas Instruments
- Radiation hardened ADC manufacturers: Maxwell, Analog Devices, S3 Group, ST Microelectronics, Texas Instruments
- Totally more than 500 components

FPGAs

- Commercial FPGA manufacturers: Xilinx, Altera
- Radiation hardened FPGA manufacturers: Xilinx, Actel, Aeroflex

ADCs and FPGAs manufacturers

SPACE-QUALIFIED ADC

Manufacturer	Part Number	Resolution [bits]	Sample rate [Msps]	Power [mW]	SNR [dB]	SINAD [dB]	SFDR [dBc]
Analog Devices							
	AD1671	12	1.25	750	69.65	68	74.5
	AD1672	12	3	363	66	63	65
	AD6645	14	80	1750	72	71.5	76
	AD9054	8	200	781	42	40	54
	AD9042	12	41	735	52	52	50
	AD9058	8	50	1040	44	43.3	50
	AD9283	8	100	120	43.5	42.5	49
Texas Instruments							
	ADS5424SP	14	105	1900	72.4	71.3	82.5
National Semiconductor							
	ADC081S101	8	1	10	49.7	49	68
Maxwell							
	9240LP	14	10	295	77	76	90
	9042	12	41	595	68	67.5	90
ST Microelectronics							
	RFH1201	12	50	100	59	56.5	57
S3Group							
	S3AD40M13BC90S	13	40	50	68	67	79

SPACE-QUALIFIED FPGAS

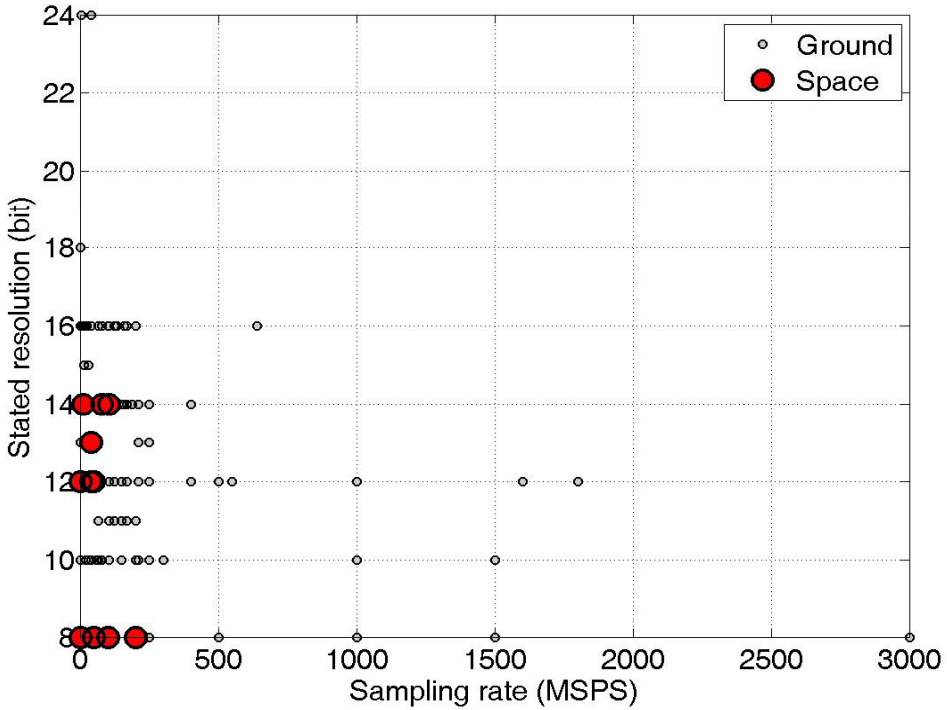
	Xilinx	Actel	Actel	Aeroflex
	Virtex 5 (FX)	RTAX-DSP	RT ProAsic 3	Eclipse
Device	SIRF	RTAX4000D	RTA3PE3000L	Eclipse
Technology	SRAM-65nm	CMOS antifuse -150 nm	Flash - 130 nm	CMOS Antifuse - 250 nm
Clock Frequency (MHz)	550	350+	250	150
Top level block combination	11200 CLBs	30 Core Tiles		
Higher level block combination	20480 Slices	8400 Superclusters		
Elementary block combination	131072 Logic Cells	16800 Clusters	75264 Tiles	
LUT number	81920	33600	75264	4002
LUT input number	6	5	3	17
Flip-flop number	81920	33600	75264	4002
DSP block number	320	120	75264	4002
Power (W) at 100 MHz	3.1 (typ.), 7.7 (max)	3.5 (typ.) and 4.2 (max)	1.4 (typ.) 1.8 (max)	1.8 (typ.) 2.5 (max)

ADCs survey

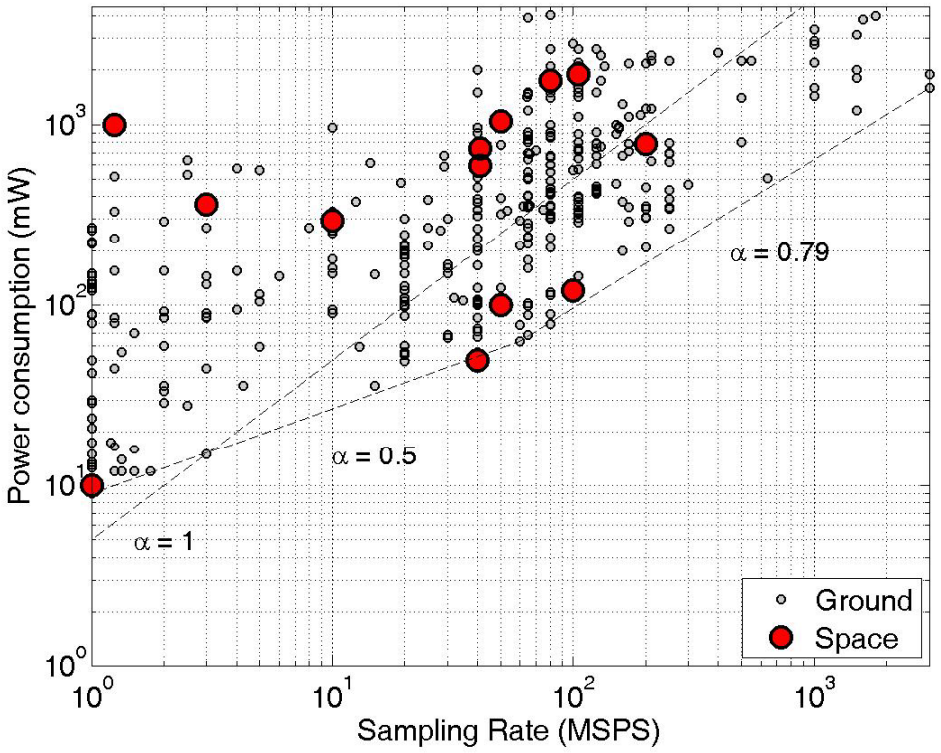
$$ENOB_{SNR} = (SNR\ (dB) - 1.76) / 6.02$$

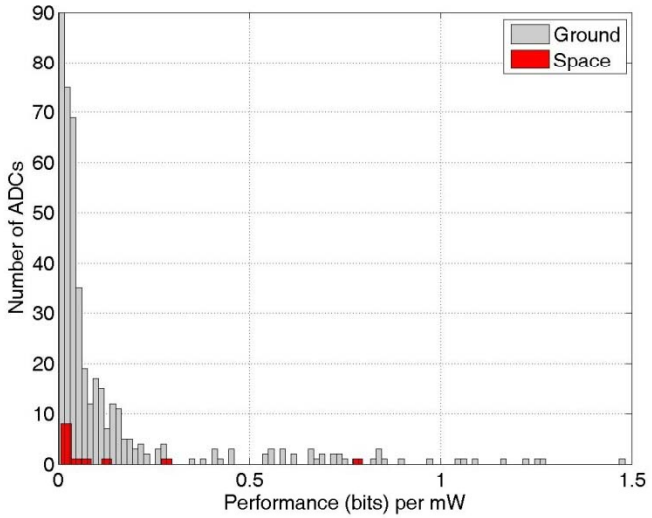
$$F = \frac{M}{P} = \frac{ENOB_{SNR} + 0.5\log_2(f_{samp})}{P}$$

$$M = ENOB_{SNR} + \frac{\log_2(f_{samp})}{2}$$

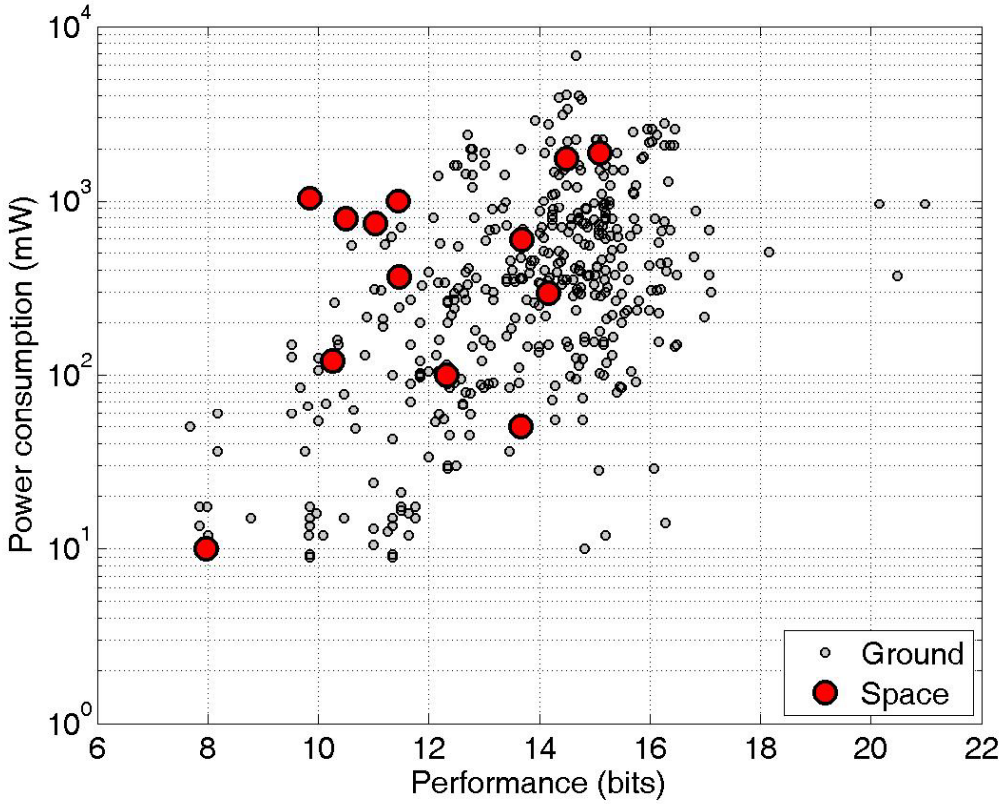


ADCs survey


Power consumption (mW)
Sampling Rate (MSPS)
α = 0.79
α = 0.5
α = 1
Ground
Space


Number of ADCs
Performance (bits) per mW
Ground
Space

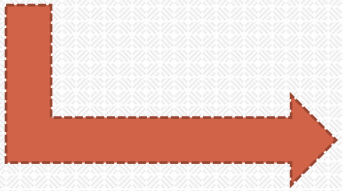
ADCs survey



ADCs survey – GEO-COMM and AISCOMM

ADC PRELIMINARY REQUIREMENTS FOR GEO-COM AND AISCOM UPLINK RECEIVER

Application	GEO-COM	AISCOM
SNR [dB]	63	54
Max Pow. cons [W]	1.3	0.4
Sampling rate [Ksps]	> 10	> 900



ADCs requirements easily satisfied by the currently available components

OVERALL TT&R RECEIVER POWER CONSUMPTION

Application	GEO-COM	AISCOM
Max tot. Power cons. [W]	13	4

ADCs survey – RF ISL

ISL AIR INTERFACE FEATURES

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Data rate [Mbps]	150
Mod. Scheme	QPSK
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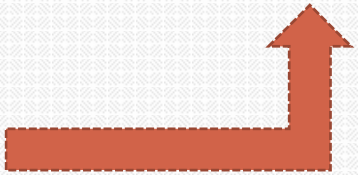
ISL ADC REQUIREMENTS

Sampling rate [Msps]	> 317.5
SNR [dB]	39.4
Max Power Cons. [W]	1.5

OVERALL ISL RECEIVER POWER CONSUMPTION

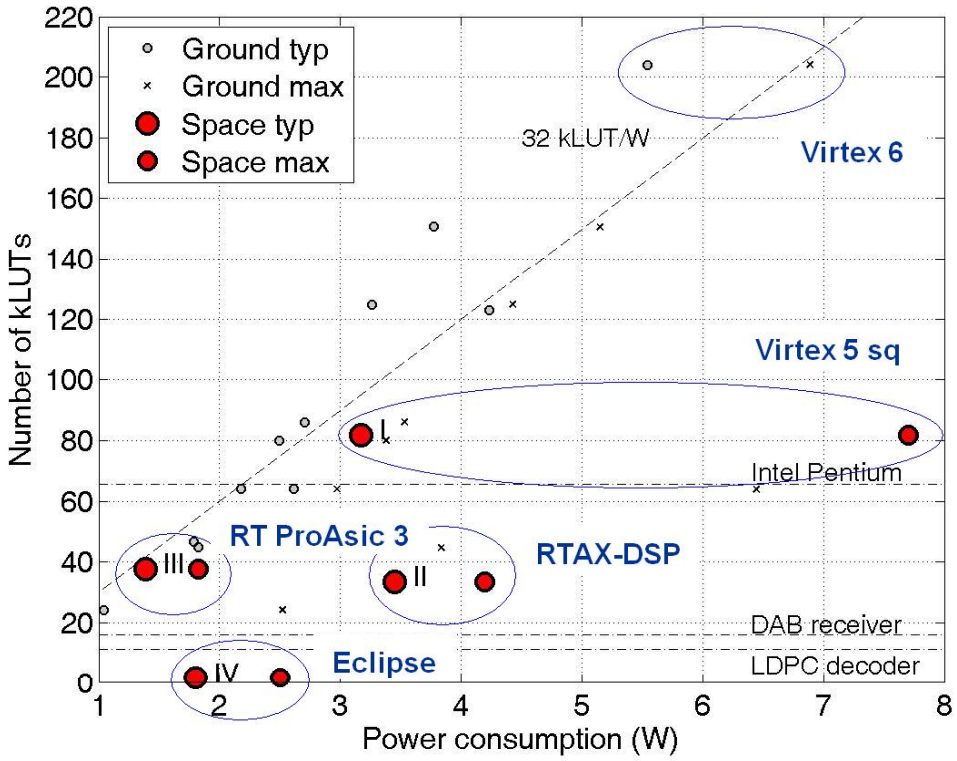
Application	LEO sat. ISL
Max tot. Power cons. [W]	15

- Not yet space-qualified components available able to fullfill them
- Possible solution for a reduced data rate



FPGAs survey

- Estimation of absolute FPGA power consumption is difficult
- Rough worst case estimate: clock frequency of 100 MHz, all logic resources (look-up tables, flip-flops, multipliers) were used on each device.



Conclusions

- Considerable market delay (ADCs)

Components	Months of difference between the commercial and the space qualified version release dates
Analog Devices	
AD1671	184
AD1672	175
AD6645	76
AD9054	80
AD9042	133
AD9058	61
AD9283	102
National Semiconductor	
ADC081S101	181
Texas Instruments	
ADS5424SP	45

- In average 9.6 years

Conclusions

- Considerable market delay

Components	Months of difference between the commercial and the space qualified version release dates
Xilinx Virtex 5	50
Actel RT ProAsic 3	28
Aeroflex Eclipse	25

- In average 2.8 years


Questions ??